FPGA-Controlled Switch-Reconfigured Antenna

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***Abstract*—In this letter, p-i-n diodes are used as switches to connect and disconnect four patch sections to a midsection of a planar antenna. The antenna system is connected to the field programmable gate array (FPGA) board controlling the activation of these switches. The antenna with the incorporated diodes is designed, installed, and measured. The methodology for using an FPGA to optimally control and produce the desired antenna frequency operation is presented and analyzed. The analogy between the measured and simulated results is found to be satisfactory. The proposed control methodology can be used with various antenna designs to obtain different possible states in an easy, fast, and low-cost manner.**

***Index Terms*—Field programmable gate array (FPGA), microstrip antennas, reconfigurable antennas.**

I. Introduction

RECONFIGURABLE antennas extend the functional possibilities of regular antennas by allowing their configurations to change on demand. The basic idea involves flexibly connecting a series of conductors together (which form the basis of the antenna) through switches that are managed under software control.

The underlying mechanisms for reconfiguration have been based on a variety of techniques. More recently, antenna designers have used electrically actuated switches and variable capacitors in order to achieve reconfiguration [1], [2]. Most antenna designers resort to RF-MEMS (microelectromechanical switches) [3] and p-i-n diodes to achieve switching, while others resort to Schottky or other types of diodes [4]. In [5], switches are used to connect different patches together. In [6], five sections of a spiral arm constituting a patch antenna are connected with four RF-MEMS. In [4], Schottky diodes bridge over a slot to achieve reconfiguration.

This letter proposes the reconfiguration of antennas through the use of p-i-n diodes that bridge conducting subsections to a main antenna section. The activation and deactivation of these p-i-n diodes is controlled through a field programmable gate array (FPGA), which manages the overall antenna configuration under software control. The use of FPGA has been previously focused in the field of smart antenna arrays [7], [8] mainly to control the beam-steering or for signal processing purposes. Here, the FPGA is used to control a single antenna that is reconfigurable. The antenna's design, structure, tuning, and the FPGA programming is investigated in the present letter. This antenna was fabricated, and the FPGA-controlled p-i-n diodes were tested. The measured results present good correlation with the simulated data.

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II. FPGAs and Reconfigurable Systems

FPGAs strive to form arbitrary digital systems (arrangements of logic, memory, and interconnects) by configuring prebuilt circuit fabrics as needed. They are based on a large number of logic cells, memory blocks, and configurable routing networks [9]. The logic cells typically implement simple Boolean functions using lookup tables (LUTs) that each implement the truth table of a logic function. LUTs can be registered with a clockable flip-flop (useful for constructing state machines) or bypassed to permit the cascadable construction of larger functions. The composition of these elements to form complex networks is achieved through programmable routing resources. These resources are large numbers of wires and switches to implement routable networks that ultimately connect to input/output (I/O) cells that form the external termini (pins) of the FPGA. While modern FPGAs feature a great variety of other additional functional blocks ("diffused intellectual property"), ranging from carry-select chains to digital signal processing (DSP) blocks and embedded complex microprocessors, the basic scheme is essentially the same. That is, FPGAs are configurable arrangements of configurable elements, the overall ensemble having the ability to represent a complex digital system.

The configuration of an entire FPGA can be represented as a large Boolean string called a *bit-stream*. Commonly, the Joint Test Access Group (JTAG) standard [10] is used as a serial configuration approach for FPGAs. While its original intent was for test monitoring (through boundary scan), it has been conveniently used to set binary signals within complex systems. A major advantage of using JTAG is that it need not interfere with circuit functions when not in testing mode. The operation of JTAG within client devices is governed through a test access port (TAP) controller module, a relatively simple finite state machine design directly embedded in the FPGA system control logic.

One of the useful features of JTAG is the ability to chain the configuration ports of several devices together and to isolate them individually for programming. Such approaches are commonly used in systems that desire the ability to use a single bit-stream source to contain the configurations for multiple FPGAs. An even more powerful interpretation can

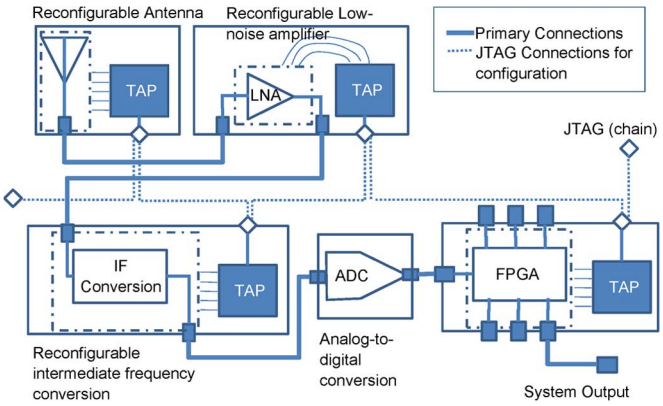

Fig. 1. Canonical reconfigurable system, based on connection of configurable and nonconfigurable components, controlled by common JTAG scan chain.

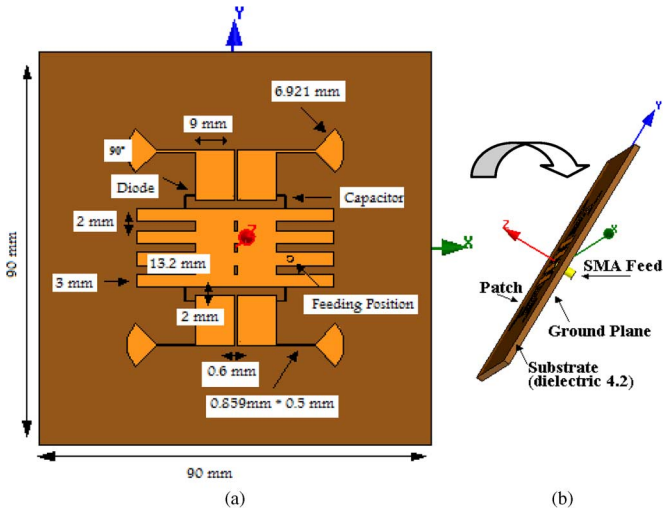

Fig. 2. (a) Front view with different dimensions. (b) Side view of the antenna.

be supported, however, which is the notion of a generalized reconfigurable system with multiple components, not all of which are FPGAs. Such a reconfigurable system is depicted notionally in Fig. 1. This system is a depiction of a prospective software-definable radio that consists of five components, of which four are reconfigurable (antenna, low-noise amplifier, IF conversion, and FPGA). The reconfigurable elements are managed through internal TAP controllers, which are accessed through a chained JTAG interface.

Reconfigurable systems of the type depicted in Fig. 1 do not currently exist, although this interpretation is straightforward. In each component, a number of digitally definable features are present, each of which is part of a configuration bit-stream that, as in the case of the FPGA, is of a format particular to the component. The bit-streams are managed through individual TAP controllers using JTAG to manage the configurations of the components individually and of the system as a whole (since its configuration is simply the concatenation of the bit-streams of individual components). While this letter does not investigate the detailed structure of a variety of possible reconfigurable building blocks, an example of how a reconfigurable antenna might be constructed is detailed in the next section.

III. Reconfigurable Antenna Structure and Tuning

The antenna structure consists of three layers; the bottom layer (90×90 mm^2) is a ground plane that covers the entire substrate. The middle substrate has a dielectric constant $\varepsilon_r = 4.2$ and a thickness of 0.235 cm. The upper layer is the metal patch composed of a main midsection and four surrounding smaller sections as shown in Fig. 2. This antenna is fed through a 50-Ω coaxial cable. The feeding position and the antenna dimensions are shown in Fig. 2(a). A side view of the antenna is shown in Fig. 2(b).

The variations in configuration are achieved through individually controllable switches, each implemented as a p-i-n diode. Microsemi's GC 4712 GaAs p-i-n diodes are used to connect the small section to the main section as shown in Fig. 2. These p-i-n diodes operate until 18 GHz and are oriented in the x-direction.

Connecting the p-i-n diodes to the main section of the antenna are 47-pF capacitors; these capacitors are oriented in the y-direction. The capacitors are used to prevent the dc current from crossing into the main section while passing the RF current. Quarter-wavelength transmission lines designed at 7.7 GHz are used to bias the p-i-n diodes. Simulations show that these copper lines resonate at a frequency where the length of the bias lines is approximately $0.45\lambda_{\text{eff}}$ and at its odd multiples, λ_{eff} being the effective wavelength at the frequency of operation. In this case, these lines resonate around 9 GHz and its odd multiples. The directions of the bias lines are also optimized to contribute constructively to the radiation pattern of the antenna that is reconfigured.

These $\lambda/4$ lines are terminated by $\lambda/4$ radial stubs in order to eliminate interference of the dc biasing network with the radiating structure. Biasing these p-i-n diodes separately can connect the corresponding side sections to the midsection, respectively. The antenna achieves multifrequency resonance tuning, which is shown in Fig. 3. Different switch configurations exhibit different S_{11} results as shown in Fig. 3. The four configurations shown in Fig. 3 represent an example of the $2^4 = 16$ possible configurations achieving frequency change. This shift is noticed at frequencies lower than 3.5 GHz, where a lot of wireless communications applications can be found, which improves the practicality of the design. In Fig. 3, "0" represents the OFF state of a diode, and "1" represents the ON.

Comparisons between the E- and H-plane cuts (yz, xz plane cuts) of the simulated and measured radiation patterns at 4.875 GHz when all the switches are OFF are shown in Fig. 4. The radiation pattern is measured at a resonant frequency common to all the antenna configurations. It is important to know that the FPGA being behind the ground plane and far from the antenna does not interfere with the antenna's radiation pattern or gain. Our experience has shown that most care should be taken in dealing with the biasing lines when it comes to any distortions to the antenna pattern. This antenna system was simulated with Ansoft HFSS ver. 11. The radiation pattern exhibits changes for different switch configurations. Fig. 5 shows the simulated E-plane cut for two different switch configurations at 2.305 GHz.

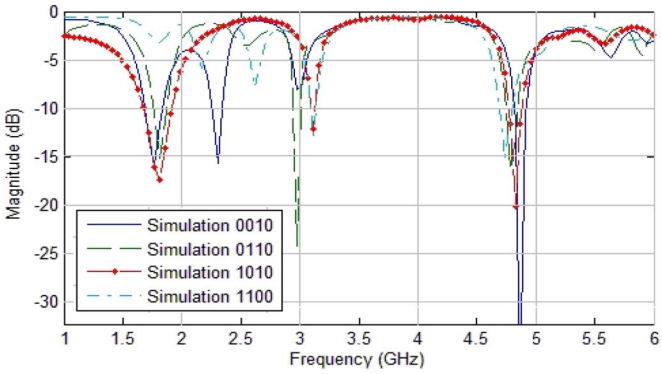

Fig. 3. Antenna resonances for different diode states: 0— OFF, 1—ON.

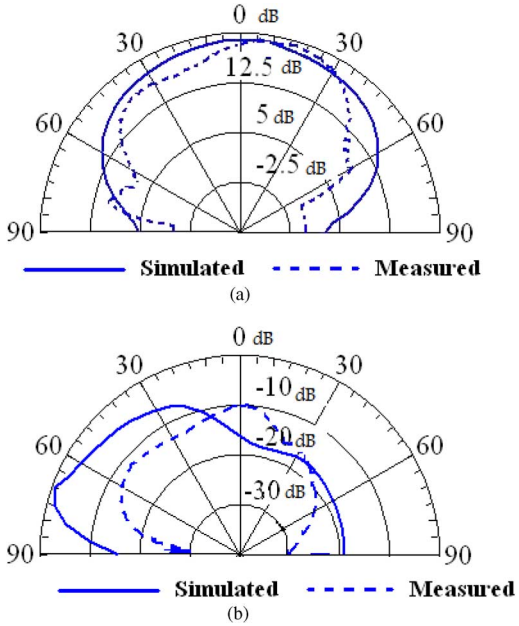

Fig. 4. Simulated and measured radiation pattern comparison at 4.875 GHz with all switches OFF: (a) E-plane cut (yz) and (b) H-plane cut (xz).

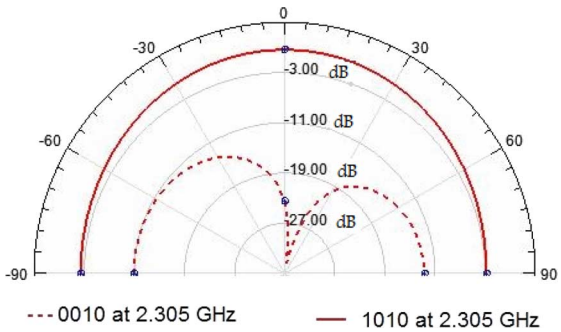

Fig. 5. Comparison between the E-plane cut (yz) of the simulated radiation pattern for two switch configurations at 2.305 GHz.

IV. Reconfigurable Antenna Fabrication, Measurement, and FPGA Control

The fabricated prototype is shown in Fig. 6. Shorting pins were inserted into 0.75-mm-diameter holes drilled at the point of intersection between the p-i-n diodes and the 47-pF capacitors. These shorting pins are used to connect the Microsemi's

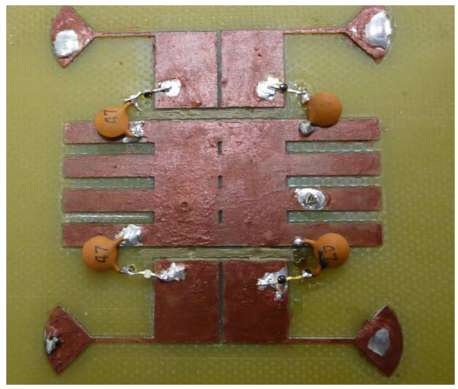

Fig. 6. Photograph of the fabricated prototype.

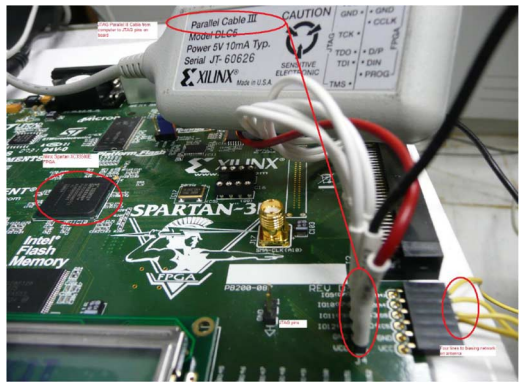

Fig. 7. The parallel III cable with FPGA board.

GC 4712 GaAs p-i-n diodes to ground. The VCC is connected to the through pins across holes drilled in the radial stubs. To implement the configuration control infrastructure for this configurable antenna, an FPGA is used to implement a TAP controller as suggested in Fig. 1. The FPGA's output lines feed the shorting pins to activate and deactivate the p-i-n diodes.

The FPGA implements a TAP controller to manage the state of these outputs using a design consistent with the IEEE 1149.1 JTAG standard [10]. A Digilent Spartan 3E board with a Xilinx Spartan XC3S500E FPGA is programmed with the TAP Controller module. A Xilinx Parallel III cable is connected from a parallel port on a Linux PC to the JTAG interface pins on the Spartan 3E board [11].

Four pins on the Spartan 3E board serve as the outputs for driving signals to the diode biasing network. The parallel III cable as well as the board is shown in Fig. 7.

The antenna reconfiguration is achieved through the following setup. A Linux computer runs the JTAG software, issuing instructions to a Spartan 3E Xilinx FPGA over a Parallel III cable. The TAP controller programmed on the FPGA translates these instructions and asserts the associated signals to bias the p-i-n diodes on the antenna. The VHDL code used to program the FPGA was assembled from [12]. With one of the p-i-n diodes biased, the RF signal passes from the main patch through the capacitor and that diode to the outer patch.

Two comparisons between the simulated and measured S_{11} results are shown in Figs. 8 and 9 for two different configuration settings, demonstrating a reasonable degree of correlation.

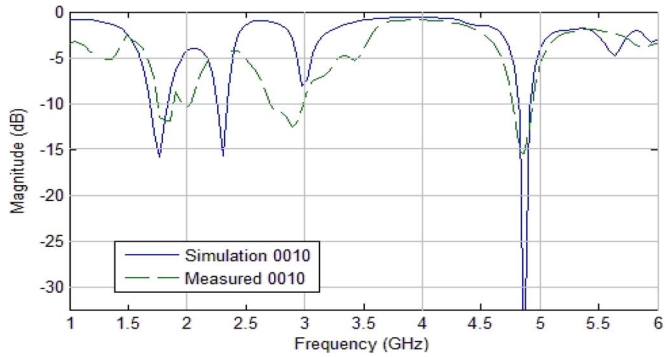

Fig. 8. Measured and simulated $|S_{11}|$ comparison for the 0010 antenna state.

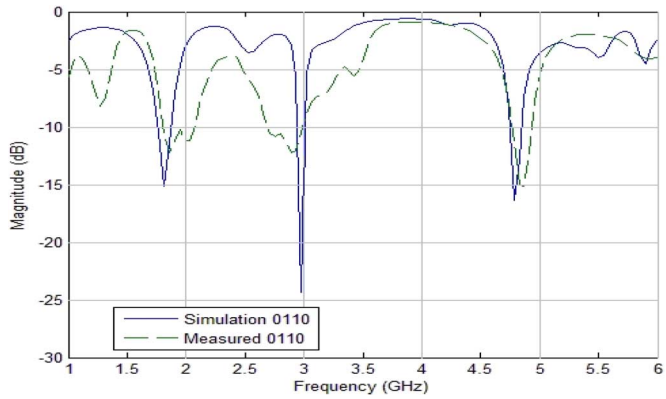

Fig. 9. Measured and simulated $|S_{11}|$ comparison for the 0110 antenna state.

V. Conclusion

In this letter, a new approach in reconfigurable systems is demonstrated using an antenna as an example of a digitally controlled component. This antenna is reconfigured using p-i-n diodes as switches. The diodes connect and disconnect four different sections of a patch to a main patch to achieve resonance tuning. The control of these p-i-n diodes is achieved through an FPGA implementing a TAP controller compliant with the popular JTAG standard.

The FPGA controlling board constitutes the lower layer of the antenna system. The antenna with the incorporated diodes is designed, fabricated, and measured. FPGAs are programmed to achieve the control process.

The ability to control reconfigurable antennas using computers and programmable devices is now feasible. This development in the automated control of reconfigurable antennas will help in the emergence of future intelligent and self-reconfigurable antenna implementations. Moreover, it is possible to combine such antennas with other existing (e.g., FPGAs) and emerging JTAG-configurable building blocks to make scalable, reconfigurable systems whose total configuration states may be software definable. These developments suggest the possibility of more flexible and capable software-definable radios, which have usually focused only on digital signal processing algorithms in FPGAs and have neglected a more expansive interpretation of reconfigurable systems.

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